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U.S. PATENT APPLICATION

for

METHOD AND APPARATUS FOR OPTICAL PROCESSING

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METHOD AND APPARATUS FOR OPTICAL PROCESSING

FIELD OF THE INVENTION

The invention relates to optical computing devices. In particular, the invention relates to hardware implementations of optical computing logic gates. The optical logic gates are configured to be used in optical processing devices.

BACKGROUND OF THE INVENTION

Optical processors function based on the action of photons in an optical circuit. The use of optical processors provide faster computation times and immunity from electromagnetic interference when compared to conventional electronic processors. However, practical implementations of optical processors have not been realized. Optical processing devices have heretofore not been miniaturized, easily mass produced, made reliable and designed to consume low power. Further, optical processing devices have not been shown to be integratable on a single substrate or to have the ability to interface with electronic systems with ease. These difficulties are due to the fact that internal representations, realizations, and implementations of logic and arithmetic units utilizing interference characteristics, interconnections, and architectures have not been realized.

Accordingly, there is a need for optical processors that may be formed on a substrate in a miniaturized form. Further, there is a need for optical processors that utilize the interference properties of light to form logic gates. Further still, there is a need for optical processors that are easily manufactured. Yet further still, there is a need for optical processors that are easily interfaced with conventional electronic devices. Yet further still, there is a need for optical processors that outperform

conventional electronic processors. Yet further still, there is a need for optical processors that are reliable and designed to consume low power.

SUMMARY OF THE INVENTION

An exemplary embodiment relates to an optical logic circuit. The optical logic circuit includes a substrate comprising a first material. The optical logic circuit comprises an optical layer overlaying the substrate at least partially comprising a second material. The optical layer is patterned to provide a plurality of optical pathways. At least one of the optical pathways is configured to transmit an optical bias. At least one of the optical pathways is configured to provide an optical input. At least one of the optical pathways is configured to provide an optical output. The optical pathways are configured to provide a Boolean logic output based on the at least one optical input.

Another exemplary embodiment relates to an optical logic gate for an optical processor. The optical logic gate includes a substrate configured of a first material. The optical logic gate also includes a Not shown patterned optical layer overlying the substrate at least partially configured of a second material. The patterned optical layer provides a plurality of optical conduits of the second material, at least one of the optical conduits is configured to receive an optical input and at least one of the optical conduits is configured to provide an optical output. The optical conduits are configured to provide a Boolean logic output based on the at least one optical input.

Yet another exemplary embodiment relates to a method of creating at least one optical logic gate. The method includes providing a substrate of a first material. The method also includes providing a second material overlying the first material. The method further includes patterning the second material by removing at least some of the second

material. The method still further includes providing a third material overlying at least the substrate.

Yet still another exemplary embodiment relates to a method of providing a Boolean logic optical output based on at least one optical input. The method includes providing light to the at least one optical input. The method also includes providing a plurality of optical pathways. Further, the method includes providing a light bias. Further still, the method includes providing an optical output, the optical output is based on the at least one input and is representative of a Boolean logic function.

Yet still another exemplary embodiment relates to an optical logic circuit. The optical logic circuit includes a substrate comprising a first material. The optical logic circuit also includes an optical layer overlaying the substrate at least partially comprising a second material. The optical layer is patterned to provide a plurality of optical pathways. At least one optical pathway is configured to provide an optical input, and at least one optical pathway is configured to provide an optical output. The optical pathways are configured to provide a Boolean logic output based on the at least one optical input.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will become more fully understood from the following detailed description, taken in conjunction with the accompanying drawings, wherein like reference numerals refer to like elements, in which:

FIG. 1 is an illustrative representation of an optical NOT (inverter) gate;

FIG. 2 is an illustrative representation of the optical NOT (inverter) gate of FIG. 1;

FIG. 3 is an illustrative representation of an optical NAND gate;

FIG. 4 is an illustrative representation of an optical AND gate;

FIG. 5 is an illustrative representation of an optical exclusive OR (XOR) gate;

FIG. 6 is an illustrative representation of a semiconductor laser;

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FIG. 7 is an illustrative representation of the cancellation of light due to constructive interference of wavefronts; and

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FIG. 8 is an illustrative representation of a cross section of an optical processing device.

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DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Referring now to FIG. 1, an exemplary embodiment of a NOT (inverter) gate 10 is depicted. Inverter gate 10 is a material patterned on a substrate, such as, but not limited to, a doped silicon or doped gallium arsenide material. Inverter gate 10 includes an optical bias input 15, optical bias input 15 configured to receive a constant light input or light bias (hereinafter, references made to light include any wavelength of electromagnetic radiation, including, but not limited to electromagnetic radiation in the visible spectrum). Inverter gate 10 further includes a second optical input 20 which selectively receives a light input. Further still, inverter gate 10 includes an interference region 25 in which light coming from inputs 15 and 20 is received. Inverter gate 10 also includes an optical output 30 that receives the optical output generated by interference region 25 based on inputs 15 and 20.

As depicted in FIG. 1, a bias light input is constantly received by bias light input 15. In the situation of FIG. 1, input 20 is dark, in other words, input 20 does not receive any light input. Interference region 25 thus receives incoming light from bias input 15. Because no other light

enters interference region 25, the light is provided through output 30, virtually undisturbed.

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As depicted in FIG. 2, light may be provided to input 20 simultaneous with the bias light provided to bias input 15. Light from bias input 15 and input 20 are received in interference region 25. Light waves in interference region 25 destructively interfere, in particular, along line 35 which is substantially aligned with output 30. Therefore, output 30 provides a substantially dark output, in other words, the energy of the light coming from interference region 25 is low, i.e., below a predetermined threshold.

The NOT gate depicted in FIGs. 1 and 2 performs a basic logic function normally called inversion or complementation, and is commonly referred to as an inverter. The purpose of the optical inverter is to convert or change one logic level to another logic level in terms of light. If a light is applied to its input, a dark will appear on its output. If a dark is applied to its input, a light will appear on its output. The operation of the inverter is summarized with Table I, which shows the output for each possible input.

Bias	Input	Output
Light	Light	Dark
Light	Dark	Light

TABLE I: Truth Table for Inverter.

The optical interference caused in interference region 25 is further depicted in FIG. 7. The optical interference may be termed an interaction of two or more light waves 70 and 75 yielding a resultant irradiance which deviates from the sum of the component irradiance. FIG. 7 depicts the action of wavefront splitting, which is one building block in optical realization of Boolean operators as used in the exemplary

embodiments. As depicted in FIG. 7, light waves 80 coming from a source 85 are received by a slit S_1 90 and slit S_2 95. Wavefronts 70 and 75 coming from slits 90 and 95 interfere at points, such as, but not limited to, point 100, thereby causing destructive interference which may be observed as interference fringes if the light is projected onto a plain screen, such as screen 110. Using, an expression associated with Young's experiment, one of ordinary skill in the art may calculate the approximate position of interference fringes on screen 110. Similarly, as applied to interference region 25, as depicted in FIGs. 1 and 2, one of ordinary skill in the art may calculate the location of output 30, such that output 30 is substantially aligned with an interference line such as line 35 (FIG. 2).

Referring now to FIG. 3, the construction of an optical NAND gate is depicted. Similar to the NOT gate of FIGs. 1 and 2, NAND gate 300 of FIG. 3 may be constructed of a material patterned on a substrate. NAND gate 300 includes a bias input 305, a selective input A 310 and a selective input B 315. NAND gate 300 further includes output 320 optically coupled to inputs 305, 310, 315, and output 320 via an interference region 325.

The NAND gate 300 is a "universal" function, that is, it can be used, alone or in combination with other NAND gates or logic gates, to construct an AND gate, an OR gate, an inverter (NOT gate), or any combination of these functions. The logic operation of optical NAND gate 300 is such that a dark output occurs only if all inputs are lighted. If any of the inputs are dark, the output will be dark.

The operation of two-input NAND gate 300 is summarized with Table II, which shows the output for each possible input combination.

Bias	InputA	InputB	Output
Light	Light	Light	Dark
Light	Light	Dark	Light
Light	Dark	Light	Light
Light	Dark	Dark	Light

TABLE II: Truth Table for Two-Input NAND.

FIG. 3 depicts a basic operation of optical NAND gate 300. In the state depicted in FIG. 3, both input A 310 and input B 315 are lighted. The wavefront interference occurs along line 330, which is in alignment with output 320. Therefore, there will be substantially little energy (light) output (i.e., the output will be dark). In an alternative state, if any of the input terminals are dark, then output terminal 320 will be light. FIG. 3 also shows a second wavefront interference line 332. Output 320 could alternatively be aligned with second wavefront interference line 332.

Referring now to FIG. 4, an exemplary embodiment of an AND gate 400 is depicted. AND gate 400 is constructed from a NAND gate 300 and a NOT gate 10 coupled to one another. An input 20 of NOT gate 10 is optically coupled to an output 320 of NAND gate 300. A bias light input 15 of NOT gate 10 is optically coupled to a bias light input 305 of NAND gate 300. AND gate 400 or NAND gate 300 and NOT gate 10 together perform the basic operation of logic multiplication commonly known as the AND function. AND gate 400 comprises two or more inputs 410 and 415, and a single output 430.

In operation, optical AND gate 400 is configured such that output 430 is light when both inputs 410 and 415 are light. If either of inputs 410 and 415 are dark, the output 430 is dark. The operation of two-input AND gate 400 is summarized in Table III, which shows the output 430 for each possible input 410 and 415 combination.

Bias	InputA	InputB	Output
Light	Light	Light	Light
Light	Light	Dark	Dark
Light	Dark	Light	Dark
Light	Dark	Dark	Dark

TABLE III: Truth Table for Two-Input AND.

For proper operation, AND gate 400 is configured with a light bias 405 that is transmitted to NAND gate interference region 425 and NOT gate interference region 426.

Referring now to FIG. 5, an exemplary embodiment of an exclusive OR (XOR) gate is depicted. Exclusive OR (XOR) gate 500 includes input A 510 and input B 515. Exclusive OR (XOR) gate 500 also includes an output 520 and an interference region 525 coupled between inputs 510 and 515 and output 520. In the state depicted in FIG. 5, a light input is transmitted through input A and input B causing interference along line 530. The interference caused along line 530 provides a substantially dark output 520. It should be noted that the XOR function does not require an optical bias input.

The operation of XOR gate 500 is summarized with Table IV, which shows the output for each possible input combination.

Input A	Input B	Output
Light	Light	Dark
Light	Dark	Light
Dark	Light	Light
Dark	Dark	Dark

TABLE IV: Truth Table for Inverter.

As depicted in FIG. 6, a semiconductor laser 600 is illustrated. Laser diodes, such as laser diode 600 may be used as a source of electromagnetic radiation or light for the optical gates as described above. Semiconductor lasers are one of many possible input interfaces to optical computing devices (in contrast, any of a variety of electromagnetic detectors may be used as output interfaces to optical computing devices). Semiconductor lasers, such as semiconductor laser 600 rely on the electroluminescence phenomenon. The electroluminescence phenomenon is the generation of light 610 by an electric field current 620 passing through a material under an applied electric field. Electroluminescent light differs from thermal radiation or incandescence in the relatively narrow range of wavelengths contained within its spectrum (for example, for a typical LED, the spectral line width is typically 100 to 150 angstroms). Further, the light may be nearly perfectly monochromatic, as in the laser diode (0.1 to 1 angstrom). Semiconductor lasers and LEDs are based on the interaction between electron and photon in a matter. Semiconductor lasers are similar to other lasers (such as the solid-state ruby laser and helium-neo gas laser) in that the emitted radiation has spatial and temporal coherence. The list of semiconductor materials that have exhibited laser action continue to grow. Table V shows the range of laser emission wavelengths for various semiconductors from near ultraviolet to far infrared. Two exemplary materials are $Al_xGa_{1-x}As_ySb_{1-y}$ and $Ga_xIn_{1-x}As_yP_{1-y}$.

A plurality of materials may be used for semiconductor lasers, including gallium arsenide and silicon materials, among many others, as provided in Table V, which is exemplary of a plurality of materials suitable for semiconductor lasers. Further, Table V illustrates corresponding emission wavelengths for each material.

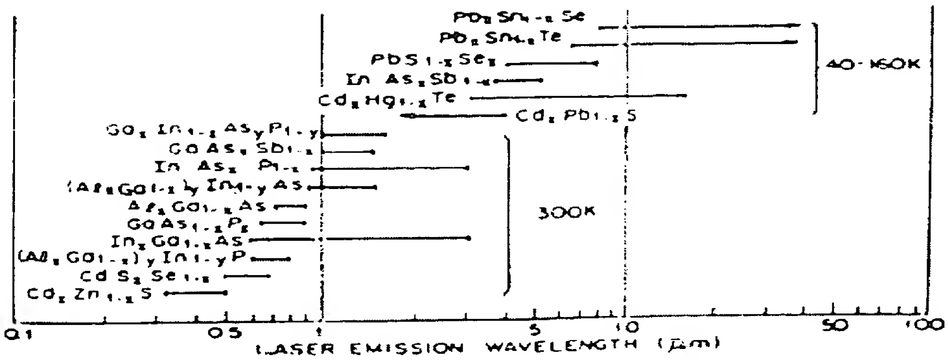

TABLE V: Semiconductor Laser Materials.

The semiconductor laser 600 of FIG. 6 shows the basic structure of a p-n junction. A pair of parallel planes 625 and 627 are cleaved or polished perpendicular to the plain of the junction. The two remaining sides 630 and 632 of diode 600 are roughened to eliminate lazing in directions other than the main direction. Diode structure 600 is called a fabry-perot cavity. As current flowing through the p-n junction is increased, radiation 610 is emitted in the main direction 608 and 609 thereby providing lazing action.

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Therefore, it is possible to construct an optical processing device having a plurality of light sources, such as lasers 600. Further, a plurality of optical gates, forming an optical processor 700, may be formed on a substrate 705, as depicted in FIG. 8. Substrate 705 (e.g., silicon, gallium arsenide, etc.) may be overlaid with a second material 710 (e.g., doped silicon, doped gallium arsenide, other nondoped materials, etc.) forming a plurality of gates patterned in second material 710. Further, the device may include a plurality of laser light sources 720 having a first layer 730 (e.g., semiconductor) overlaid with a second layer 740 (e.g., semiconductor) and having a doped junction 750

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therebetween. In an exemplary embodiment, optical processor 700 may include a non-translucent layer 760 overlaying substrate 705 and patterned gate structures 710 and semiconductor laser 720, and any other devices formed on substrate 705.

In an exemplary embodiment, a plurality of techniques often applied to forming conventional electrical semiconducting devices may be used to form optical processing devices, such as optical processor 700. For example, optical processor 700 may be formed on a silicon substrate 705. Methods used for doping and conventional semiconductor integrated circuit devices may be used to dope layer 710. Further, layer 710 may be patterned by a number of conventional techniques, including, but not limited to, photoresist techniques and etching techniques. Similarly, the formation of semiconductor laser 720 may be provided using similar techniques. Further still, a number of deposition techniques may be used to overlay layers of materials, such as material 710 and material 760 which may be done using techniques, including, but not limited to, chemical vapor deposition (CVD) techniques, and sputtering techniques. Although integrated circuit forming techniques may be utilized in forming optical processor 700, any of a variety of other techniques to form optical processor 700 may be used.

While the exemplary embodiments refer to optical processors for optical computing, the exemplary embodiments may also be applied to any of a variety of devices using optical logic gates. Further, while the exemplary embodiments refer to specific material being used, the exemplary embodiments are to be interpreted broadly. The embodiment may encompass those situations in which any of a variety of materials is used to produce the optical processing devices.

Further still, those who have skill in the art will recognize that the exemplary embodiments are applicable with many different hardware configurations, software architectures, light sources, and organizations or processes.

While the detailed drawings, specific examples, and particular formulations given describe exemplary embodiments, they serve the purpose of illustration only. The materials and configurations shown and described may differ depending on the chosen performance characteristics and physical characteristics of the optical processors. For example, the type of materials or wavelength of light used may differ. The systems shown and described are not limited to the precise details and conditions disclosed. Furthermore, other substitutions, modifications, changes, and omissions may be made in the design, operating conditions, and arrangement of the exemplary embodiments without departing from the scope of the invention as expressed in the appended claims.